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10/663,877	09/16/2003	Michael Dean Kalan	03AB088	3100

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Susan M. Donahue
Rockwell Automation
1201 South Second Street
Milwaukee, WI 53204

EXAMINER	
SCHELL, JOSEPH O	

ART UNIT	PAPER NUMBER
2114	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,877	KALAN ET AL.	
	Examiner	Art Unit	
	Joseph Schell	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *22 and 31* is/are allowed.

6)☒ Claim(s) *1-7,9,11-14,18-21,23-26 and 28* is/are rejected.

7)☒ Claim(s) *2,8,10,15-17,27,29 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Claims 1-31 have been examined.

Claims 8, 10, 15-17, 27 and 29-30 have been objected to as containing allowable subject matter, yet dependant upon rejected base claims.

Claims 22 and 31 are allowable.

Claims 1-7, 9, 11-14, 18-19, 20-21, 23-26 and 28 have been rejected.

Claim Objections

1. Claim 1 line 6 should read "a second processing unit having a second processor..."

Claim 5 line 1 should read "primary and second processing units..."

Claim 7 line 4 should read "primary and partner processing units' execution" (apostrophe being after the S).

Claim 28 line 2 should read "primary processing unit only and transfers the safety..."

Allowable Subject Matter

+29-30

1. Claims 8, 10, 15-17, and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

2. Claims 19, 20 and 25 have been rejected as described below, but contain novel limitations.

3. Within claims 8, 10, 27 and rejected claim 25, when considered within the claim as a whole, the examiner deems the novel limitation to be that the safety program is a fixed set of instructions that are repeatedly executed.

4. Within claim 15, when considered within the claim as a whole, the examiner deems the novel limitation to be the first processor of the primary unit has memory that is only indirectly accessible by the second processor of the primary unit, while the second processor of the second unit has memory that is only indirectly accessible by the first processor of the second unit.

5. Within claims 16-17, and rejected claim 20, when considered within the claim as a whole, the examiner deems the novel limitation to be that the shadow processor does not receive or execute code independently while the primary processor is in an independent mode.

6. Within claim 29, when considered within the claim as a whole, the examiner deems the novel limitation to be one processor requesting a program from the other by an identification value held within the program.

7. Within claim 30 and rejected claim 19, when considered within the claims as a whole, the examiner deems the novel limitation to be the storing of standard program data within the shadow processor memory.

8. Claims 22 and 31 are allowable.

9. Within claim 22, when considered within the claim as a whole, the examiner deems the novel limitation to be that the shadow processor does not receive or execute code independently while the primary processor is in an independent mode.

10. Within claim 31, when considered within the claim as a whole, the examiner deems the novel limitation to be the loading of data relevant to the standard program onto the partner processing unit.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 3-4,19-20 and 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. Claims 3 and 4 recite the limitation "the communications bus" in the first line of each claim. There is insufficient antecedent basis for this limitation in the claim. Examiner assumes claims 3 and 4 are instead dependent on claim 2, which does recite this limitation.

13. Claim 19 recites the limitation "the standard data" in the second line of the claim. There is insufficient antecedent basis for this limitation in the claim. Examiner assumes claim 19 is instead dependent on claim 18, which does recite this limitation.

14. Claim 20 recites the limitation "the logical combination" in the third line of the claim. There is insufficient antecedent basis for this limitation in the claim.

15. Claim 25 recites the limitation "each repeated execution" in the third line of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

16. Claims 1, 9, 11 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Hofstee (US Patent 6,751,749).

17. As per claim 1, Hofstee ('749) discloses a safety controller comprising:

a primary processing unit having a first processor communicating with a first memory (column 4 lines 1-3) holding a safety program requiring a first reliability of operation (column 4 lines 59-63 describe a program that is used to generate and compare a signature) and a standard program (column 6 lines 55-57 and column 9 lines 18-22 mention that the two processors may operate independently which would require at least a second program, one for each processor) requiring a second reliability of operation less than the first reliability of operation (when operating independently, no signatures are checked; thus this program is less reliable);

a second processor having a second processor independent from the primary processing unit and communicating with a second memory independent from the first memory and holding the safety program and not the standard program (see Figure 4,

element 434A, each processor contains an instruction cache; this cache will contain the safety program when running in reliability mode, and when operating independently it will contain programs independent of the other processor's programs); and

a synchronization program executable by the primary and partner processing units to execute the standard program in the primary processing unit only and to execute the safety program in the primary and second processing units and to compare execution of the safety programs to enter a safety state when this execution differs (column 4 lines 59-60 mentions the compare unit and column 1 lines 36-48 describes possible compare mismatch actions).

18. As per claim 9, Hofstee ('749) discloses the safety controller of claim 1 wherein the safety program executes to generate values of internal variables and wherein the synchronization program compares execution of the safety program by comparing values of internal variables generated by the primary and partner processing units executing the safety program (column 2 lines 32-38, values are computed by each processor and moved to a special register for comparison).

19. As per claim 11, Hofstee ('749) discloses the safety controller of claim 1 wherein the primary processing unit includes only a single processor (column 2 lines 30-32).

20. As per claim 23, this is a method version of limitations expressed in claim 1 and is rejected on the same grounds as claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hofstee ('749) in view of Sachs (US Patent 5,829,037) and Khan (US Patent 5,948,087).

Hofstee ('749) discloses the safety controller of claim 1. Hofstee ('749) additionally mentions the possibility of processor sparing in the event of an error (column 1 lines 45-48). Hofstee ('749) does not expressly disclose the safety controller where the processing units are in separate independent housings and a serial bus allows intercommunication between housings.

Sachs ('037) teaches a system that uses a bus for communication between processors in a multiprocessor system (column 1 lines 15-17).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Hofstee ('749) such that the processors communicate over a common bus. This modification would have been obvious because it allows

each processor to track the operations of the other when accessing shared memory (Sachs ('037) column 1 lines 22-24).

Khan ('087) teaches a system that uses a special motherboard design such that a logic board is easily removable from the system (see abstract).

At the time of invention it would have been further obvious to a person of ordinary skill in the art to modify the system disclosed by Hofstee ('749) in view of Sachs ('037) such that the processors are located on separate housings. This would have been obvious because Hofstee ('749) mentions copying a failed processor image to a spare processor (column 1 lines 45-49) and an architecture that separates components allows for easy installation, replacement and upgrade of the components (Kahn ('087) column 2 lines 4-7).

22. Claims 3 and 4 are rejected as being unpatentable over Hofstee ('749) in view of Sachs ('037) and Kahn ('087) as applied to claim 2, and in further view of PCI Express.

23. As per claim 3 Hofstee ('749) in view of Sachs ('037) and Kahn ('087) discloses the safety controller of claim 2. Hofstee ('749) in view of Sachs ('037) and Kahn ('087) additionally discloses the system wherein the processors are detachable from the communication bus (Kahn ('087) column 2 lines 32-33).

Hofstee ('749) in view of Sachs ('037) and Kahn ('087) does not expressly disclose the safety controller wherein the communication bus is a backplane.

PCI Express teaches that many systems use a CompactPCI architecture for backplane implementation (see section on Communications Systems, second paragraph).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Hofstee ('749) in view of Sachs ('037) and Kahn ('087) such that the interprocessor communication occurs over a blackplane. This modification would have been obvious because high end communication systems use a midplane or backplane chassis to interconnect multiple subsystems (PCI Express, section on Communications Systems, second paragraph).

24. As per claim 4, Hofstee ('749) in view of Sachs ('037) and Kahn ('087) discloses the safety controller of claim 2. Hofstee ('749) in view of Sachs ('037) and Kahn ('087) discloses the system wherein the processors communicate over a parallel bus (Sachs ('037), see abstract) and where subsystems are detachable from the bus (Kahn ('087) column 2 lines 32-33).

PCI Express teaches some background information about the development of a PCI Express bus.

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Hofstee ('749) in view of Sachs ('037) and Kahn ('087) such that a serial bus is utilized for the interprocessor communication network. This modification would have been obvious because the trend if PC bus technology is a move towards new, high-speed serial buses because parallel buses are reaching their practical limitations for offering increasing bandwidth (PCI Express, Scope section, third paragraph).

25. Claim 5, 7, 12, 14, 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hofstee ('749) in view of Kawano (US Patent 5,361,366).

26. As per claim 5, Hofstee ('749) discloses the safety controller of claim 1. Hofstee ('749) does not expressly disclose the safety controller wherein the primary and partner processing units are in a single housing.

Kawano ('366) teaches a multiprocessor system wherein multiple processors exist within a single housing (as shown in figure 1a).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the shadow-processing system disclosed by Hofstee ('749) such that both processors are within a single housing unit as taught by Kawano ('366). This modification would have been obvious because, while isolated processors are suitable

for a large-scale on-line computer system (Kawano ('366) column 1 lines 65-67), parallel-operating plural processors employed within a conventional computer allow for high-speed processing operations to be realized (Kawano ('366) column 2 lines 3-8).

27. As per claim 7, Hofstee ('749) discloses the safety controller of claim 1 wherein the synchronization program compares execution of the safety program by comparing outputs generated by the primary and partner processing units' execution of the safety program (column 4 lines 41-48, signatures are generated for comparison). Hofstee ('749) does not expressly disclose the safety controller wherein the safety program executes to generate outputs to be used to control an external device.

Kawano ('366) teaches a multiprocessor system with an attached printer and disk (see figure 1). At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Kawano ('366) such that the safety program causes the system to print or store results of the redundant operation mode. This modification would have been obvious because it is well known in the art to either store error logs to disk or print them for later analysis.

28. As per claim 12, Hofstee ('749) discloses the safety controller of claim 1. Hofstee ('749) does not expressly disclose the safety controller wherein the primary processing unit includes at least two processors.

Kawano ('366) teaches a multiprocessor system wherein multiple processors exist within a single housing (as shown in figure 1a).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the shadow-processing system disclosed by Hofstee ('749) such that the primary unit consists of multiple parallel processors as taught by Kawano ('366). This modification would have been obvious because, while isolated processors are suitable for a large-scale on-line computer system (Kawano ('366) column 1 lines 65-67), parallel-operating plural processors employed within a conventional computer allow for high-speed processing operations to be realized (Kawano ('366) column 2 lines 3-8) when the primary unit is operating independently.

29. As per claim 14, Hofstee ('749) in view of Kawano ('366) discloses the safety controller of claim 12 wherein the processors of the primary processing unit have independent memories (as shown in Figure 2b).

30. As per claim 24, this is a method version of limitations expressed in claim 7 and is rejected on the same grounds as claim 7.

31. As per claim 26, this claim is dependent on claim 24 and expresses limitations found in claim 9, which has been shown to be anticipated by Hofstee ('749). This claim

is therefore also disclosed by Hofstee ('749) in view of Kawano ('366) as applied to parent claim 24.

32. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hofstee ('749) in view of Heinemann (US Patent 4,388,695).

Hofstee ('749) discloses the safety controller of claim 1. Hofstee ('749) does not expressly disclose the safety controller wherein the first memory includes at least a portion that is lockable by hardware against writing.

Heinemann ('695) teaches a memory that requires a special sequence of memory accesses before allowing access to certain critical data (see abstract).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the shadow-processor system disclosed by Hofstee ('749) such that it includes the memory protection scheme taught by Heinemann ('695). This modification would have been obvious because systems occasionally crash (Heinemann ('695) column 1 lines 19-26) and a crash might cause the system to jump to an instruction causing it to overwrite critical information (Heinemann ('695) column 1 lines 26-42).

33. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hofstee ('749) in view of Kawano ('366) as applied to claim 12, and in further view of Borkenhagen (US Patent Application Publication 2003/0163642).

Hofstee ('749) in view of Kawano ('366) discloses the safety controller of claim 12. Hofstee ('749) in view of Kawano ('366) does not expressly disclose the safety controller wherein the processors of the primary processing unit share a common memory.

Borkenhagen ('642) teaches a multiprocessor system with shared memory (see abstract).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the shadow-processor system disclosed by Hofstee ('749) in view of Kawano ('366) such that the processors within the primary unit have a shared memory. This modification would have been obvious because shared memory allows all processor to access the main memory and enables the tasks of one processor to efficiently and easily shared data with another (Borkenhagen ('642) paragraph 8).

34. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hofstee ('749).

As per claim 18, Hofstee ('749) discloses the safety controller of claim 1. In the system disclosed by Hofstee ('748) the cache only expressly holds instructions. Hofstee ('749) does not disclose the system wherein the first memory also holds standard data used or generated by the standard program and safety data used or generated by the safety program and wherein the second memory holds the safety data used or generated by the safety program (the memory being each processor's cache.

At the time of invention it would have been obvious to a person of ordinary skill in the art to include a data cache for each processor along with the instruction cache. This would have been obvious because it is well known in the art that a cache will decrease data access time.

35. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hofstee ('749) in view of Kidder (US Patent 6,694,450).

Hofstee ('749) discloses the method of claim 23. Hofstee ('749) does not explicitly disclose the method wherein the safety controller receives the standard program and the safety program at the primary processing unit only and transfers the safety program only to the partner processing unit.

Kidder ('450) teaches a multiple processor system of backup processors (see abstract). Within the system, a program may load from memory to a first processor, and from the first processor to a second processor (column 18 lines 4-7).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the shadow-processor system disclosed by Hofstee ('749) such that a program loads from memory to a first processor, which then transfers it to a second processor instead of the second processor loading it from memory directly. This modification would have been obvious because downloading of the program from a coprocessor is quicker than from a central memory controller (Kidder ('450) column 18 lines 7-9).

Conclusion

The prior art made of record on accompanying PTO 892 form and not relied upon is considered pertinent to applicant's disclosure. Specifically, Quach ('313) teaches a system where two processors may either operate independently or redundantly, and Prabhu ('398) teaches a system wherein multiple processors run a test program an execution is compared.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Schell whose telephone number is (571) 272-8186. The examiner can normally be reached on Monday through Friday 9AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER